QUARTERLY REPORT NO. 6
FOR
ANALOG-TO-DIGITAL CONVERTER
CONTRACT NO. N00014-87-C-0314
1 JULY 1988 - 30 SEPTEMBER 1988

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Contract No.:	N00014-87-C-0314
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QUARTERLY REPORT NO. 6

FOR

ANALOG-TO-DIGITAL CONVERTER

Contract No. N00014-87-C-0314

1 July 1988 - 30 September 1988

I. SUMMARY

A. Brief Program Definition

This is a research and development program to design and fabricate both a GaAs high sampling rate A/D converter and a high resolution GaAs A/D converter.

B. Process Development

Much progress has been made during the past quarter. We now routinely fabricate lots with good transistor gains. A problem with the emitter ohmic metal process was identified and eliminated: The emitter ohmic contact metal was spiking through the emitter cap layer and forming a Schottky diode with the underlying base. The resulting Schottky diode effectively shorted out the base-emitter junction at low current levels. We have eliminated the problem by using a barrier layer between the Au/Ge/Ni ohmic contact layer and the subsequently deposited thick Au layer to prevent this final Au layer from interacting with the underlying GaAs. Despite this progress, however, the contact resistance continues to be unacceptably high. The barrier metal is not believed to contribute to the high contact resistance, since test lots without the barrier yield essentially the same contact resistance. Efforts are under way to improve the contact resistance by utilizing the new barrier layer metal system. This problem is being addressed by running split lots in the GaAs pilot lines as well as by reevaluating our contact process in the development lab.

The second ADC shipped to Hughes yielded functional sample-and-hold circuits on all three wafers and for all four sample-and-hold circuit designs. For the least aggressive design the wafer yield was 50% and the lot yield was 39%. The HBTs used the barrier layer as part of the emitter ohmic process and exhibited good current gains. Despite these good gains, ADC

circuit yield is still zero because of the high emitter contact resistance.

C. Design and Test

During the past quarter, Hughes has directed its efforts toward sample-and-hold (S/H) testing and device characterization. Two HBT lots have been evaluated, one processed in June and the other in August. Although neither lot yielded any functional five-bit or four-bit ADCs, sample-and-hold (S/H) yield was quite good on the August lot . Hughes completed dynamic evaluation of several functional S/H die from the June lot. Operation of the S/H circuit at a sample rate of 500 megasamples-per-second (Msps) was achieved.

Hughes completed a brief dc characterization of the 7 x 7 μm^2 emitter HBT devices used to fabricate the S/H and ADC circuits on the August lot. It was found that the devices have extremely high and nonuniform contact resistances, an order of magnitude larger than the values used for computer simulation of the ADC circuits in January. Circuit simulations performed on the five-bit and four-bit quantizers this quarter indicate the high device contact resistances correlate with the 0% ADC yield attained thus far.

To improve the yield of the four-bit and five-bit ADCs, Hughes will redesign both ICs for improved sensitivity to high device contact resistances. The revised mask set will be released for processing in November.

II. HETEROJUNCTION BIPOLAR PROCESS DEVELOPMENT

A. Baseline Process Development

The overgrowth epitaxial process in which the emitter epi layers are grown using MOCVD over a preprocessed wafer routinely yields transistors with good current gains. Both the grown base (in which the base layer is grown as part of the first epi and then selectively etched from the field areas) and the implanted base result in good quality second-epi layers and reasonable transistors. Our current pre-epi clean-up process has eliminated the occasional poor quality second-epi layers obtained during the early stages of the overgrowth process development.

The lead ADC lot was completed on schedule and shipped to Hughes for testing. This lot contains a titanium diffusion barrier between the standard AuGe/Ni ohmic contact metal and the subsequently deposited gold layer. These four films are deposited without breaking vacuum. The 1000 Å titanium layer is designed to prevent the top gold layer from diffusing through the emitter cap layer and the AlGaAs emitter layer to form a Schottky diode with the underlying base layer. The titanium film has greatly improved control of the base-emitter turn-on voltage and has been added to our standard process. This process improvement has resulted in good yields on our S/H circuits on the latest lot, as indicated in the section below.

In addition to using a diffusion barrier as part of the n-ohmic process, TI is now processing lots that use a thicker cap layer in conjunction with the titanium. The impact of this thicker cap layer will be evaluated when the lots are completed, but initial in-process hand-probing of these lots has shown little improvement.

The most recent test lots have used titanium nitride (TiN) instead of titanium as the diffusion barrier. Titanium nitride is reported to be a better diffusion barrier than titanium or even TiW, which is the diffusion barrier used as part of our double-level metal system. The TiN is formed by evaporating titanium in a nitrogen ambient. Depending on the nitrogen partial pressure and the titanium deposition rate, the resulting film can vary from pure titanium to TiN. The films we are currently evaluating are about 30% TiN. They result in very smooth morphology in the contacts after the AuGe/Ni is sintered at 450°C.

Although the diffusion barrier has eliminated the metal spiking problem, as indicated by the good S/H circuits, high contact resistance continues to be a problem. The high contact resistance (~ 10^{-4} to 10^{-5} ohm-cm^2) is not believed to be associated with the changes made to eliminate metal spiking, since material both with and without the barrier layer exhibits high contact resistance. We are addressing this problem by running split lots in the GaAs pilot lines and reevaluating our contact process. Rutherford backscattering has been used to examine the Au/Ge-Ni interfacial layers to ensure mixing. The various ohmic metal profiles are shown in Figure 1. For

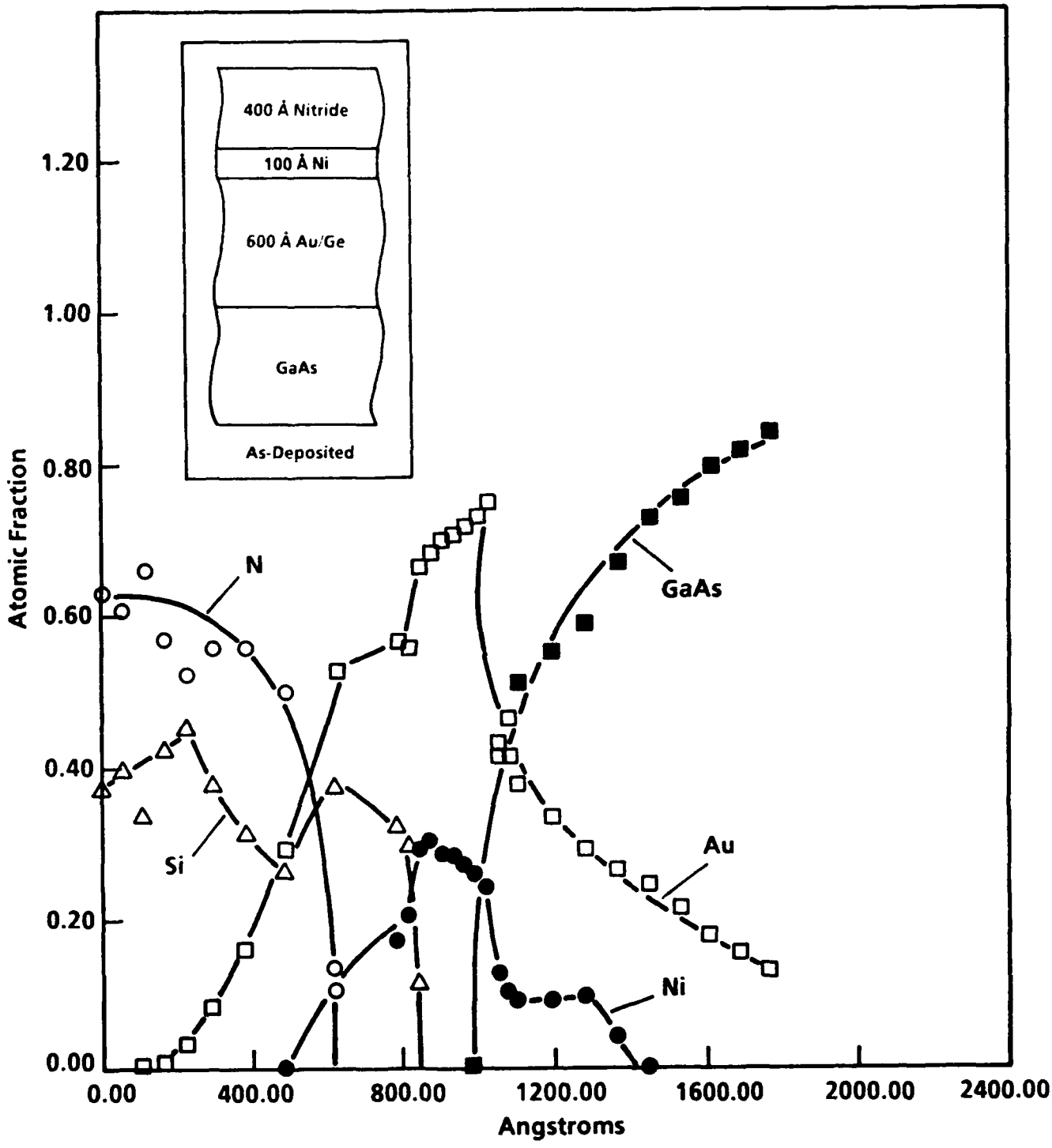


Figure 1. Rutherford backscattering n-ohmic metal profiles.

this test, the top layer of thick Au was omitted so that we would not have to ion-mill through it. A 400 Å nitride layer was used to cover the thin metal films during the 450°C anneal. The profiles appeared normal, with no interfacial layer preventing the metal-GaAs interaction. The Ge profile was not detectable by this means because of signal interactions from the other metal species. Both x-ray spectroscopy and neutron activation studies have been undertaken to ensure that the Ge doping in the Au/Ge deposited films is at the desired 12% level.

B. Circuit Testing Process

During the past quarter, Hughes completed wafer-level testing of the five-bit ADC test bar wafers received in June and August 1988. No functional five-bit or four-bit ADCs were found on either lot. However, a significant increase in the functional yield of S/H circuits was achieved with the August lot, which contained a titanium diffusion barrier for improved device yield and current gain. Yield of the two S/H versions that use only 7 x 7 μm^2 emitters increased significantly, from 2% to more than 36%, from the June to the August lot. The S/H yield results for the two lots are summarized in Table 1.

Wafer maps showing S/H functional yield improvement (four versions) for the two lots are illustrated in Figures 2 and 3. Yield statistics for the four S/H versions on the August lot are summarized in Table 2. The three HBT wafers (83-B, 83-E, and 84-B) provided a total of 66 device sites. S/H versions 2 and 4 have functional yields of 33% and 39%, respectively. These circuits predominantly use devices with 7 x 7 μm^2 emitter geometries. S/H versions 1 and 3 have functional yields of only 8% and 2%, respectively. The lower yield S/H versions use devices with 5 x 5 μm^2 emitter geometries. Table 3 summarizes the devices used among the four S/H versions.

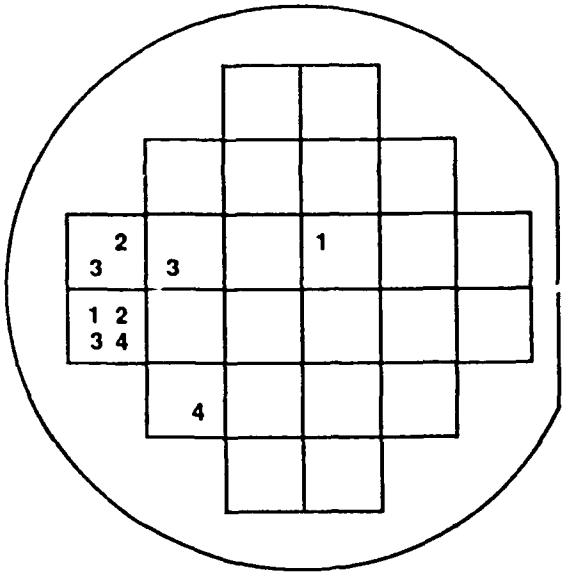
Key dc parameters were measured at wafer probe, including power supply currents, input offset voltage, gain, and track/hold isolation. The input/output transfer functions of the gate and overall S/H were measured, and a least-squares fit routine was used to determine each component's dc linearity. Graphs of dc linearity and track-mode gain for S/H version 4 on the August lot are presented in Figure 4. All functional parts are shown

Table 1

Sample-and-Hold (S/H) Yield Improvement

from June to August 1988 Lots

HBT Lot	S/H With 7 μm x 7 μm Emitter Devices		S/H With 5 μm x 5 μm Emitter Devices	
	# Functional	% Yield	# Functional	% Yield
Baseline 6/88 (144 sites)	3	21	7	4.9
With Titanium Diffusion Barrier 8/88 (132 sites)	48	36.4	6	4.5



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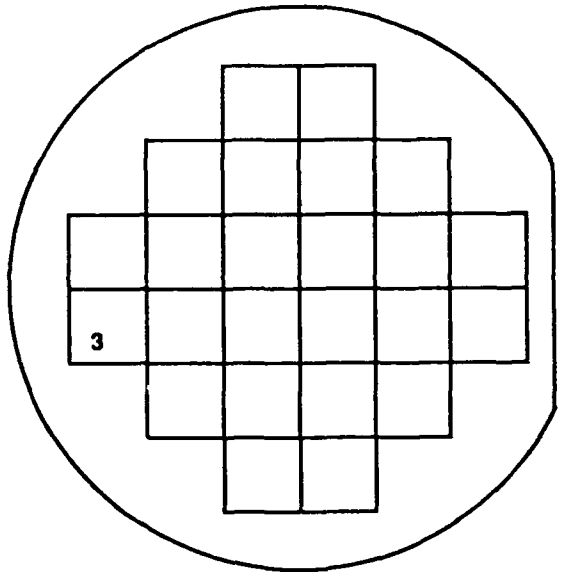

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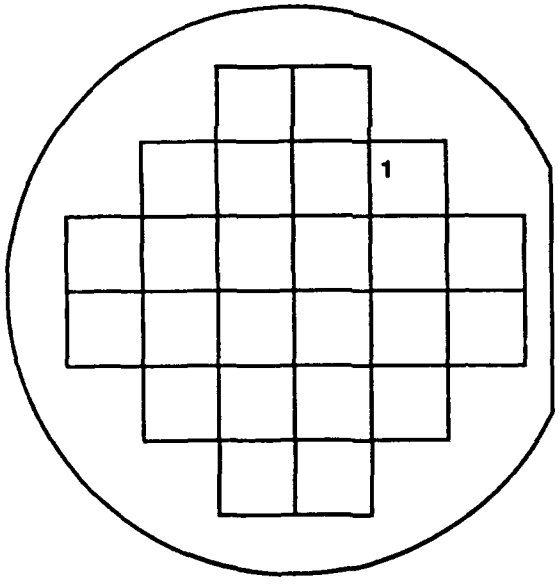

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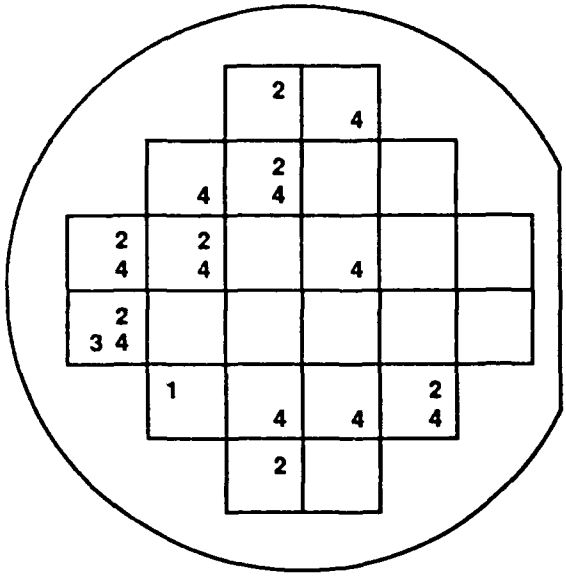
Figure 2. Wafer maps showing sample-and-hold functional yield (four versions) from June 1988 lot.



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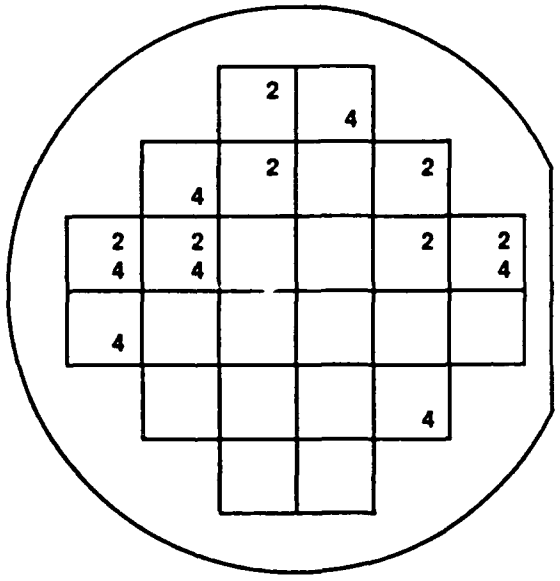

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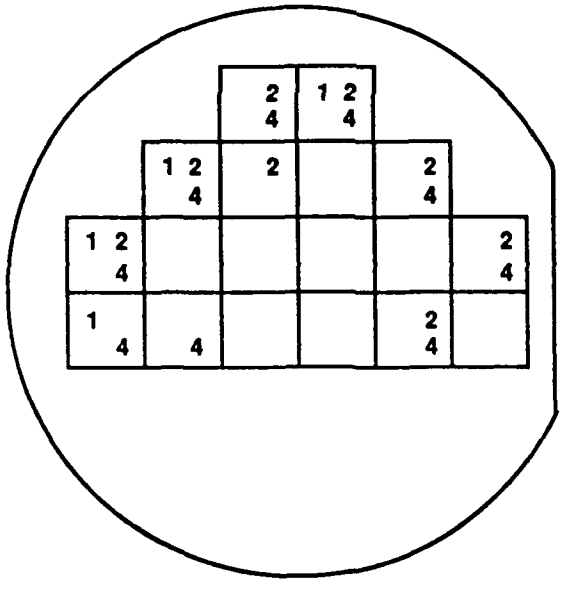


WAFER 83-E

Figure 3. Wafer maps showing sample-and-hold functional yield improvement (four versions). Wafers are August 1988 lot using titanium metal diffusion barrier.

Table 2

Sample-and-Hold (S/H) Yield Statistics from August 1988 Titanium Metal Diffusion Barrier Lot

Wafer #	S/H 1		S/H 2		S/H 3		S/H 4	
	# Functional	% Yield	# Functional	% Yield	# Functional	% Yield	# Functional	% Yield
83-B	1	4	7	29	1	4	10	42
84-B	0	0	7	29	0	0	7	29
83-E	4	22	8	44	0	0	9	50
Totals by S/H Version	5	8	22	33	1	2	26	39

Table 3

HBT Devices Used in Four Sample-and-Hold (S/H) Versions

Devices Used	S/H Versions			
	S/H 1	S/H 2	S/H 3	S/H 4
5 x 5 μm Bipolar Transistor	●		●	
7 x 7 μm Bipolar Transistor		●		●
5 x 5 μm Bipolar Diode	●			●
5 x 5 μm Schottky Diode		●		
3 x 3 μm Schottky Diode			●	

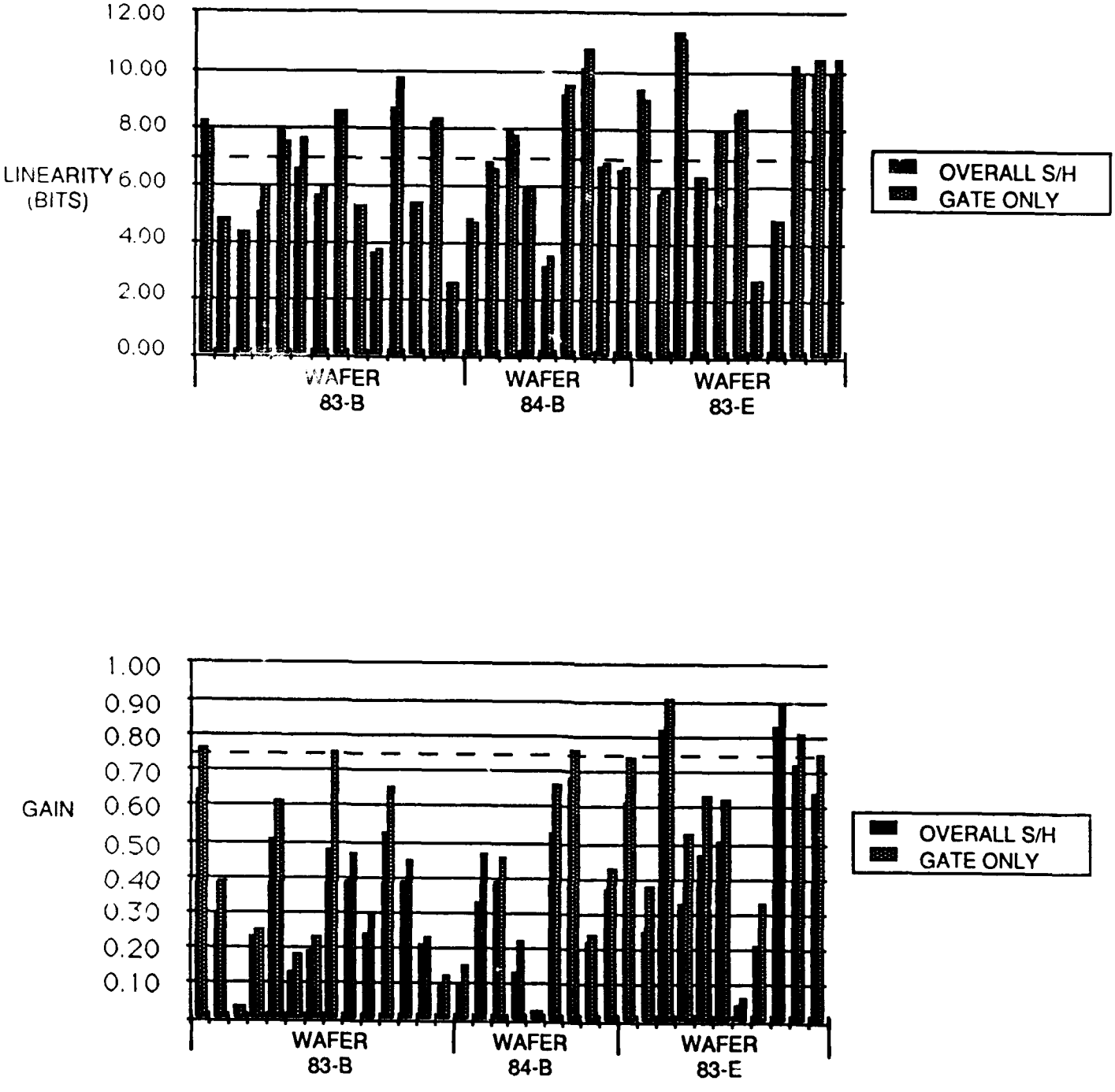


Figure 4. Wafer-level probe results for all "functional" S/H version 4, sorted by wafer. Dc linearity and gain are shown for the overall S/H and the sampling gate only.

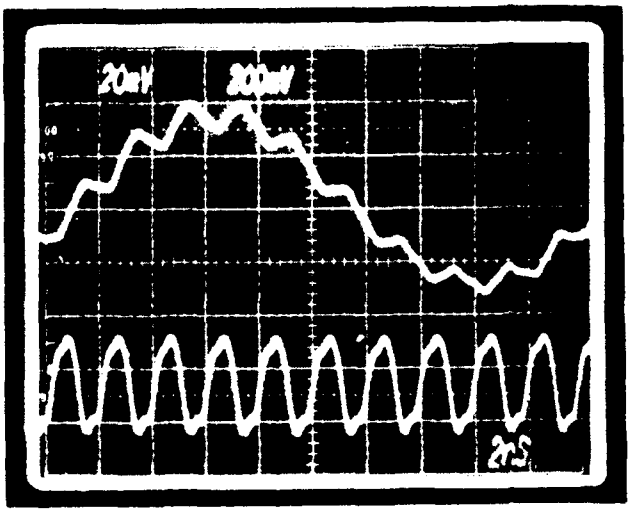
sorted by wafer number. The dashed lines on each graph represent minimum performance requirements to meet the program goals.

The three June wafers that contained functional S/Hs were diced by TI and returned to Hughes for dynamic evaluation at the end of August. Dynamic testing of the S/Hs was completed by Hughes during September. S/H dynamic parameters, including droop performance, harmonic distortion, and settling performance, were measured by Hughes in the custom test hybrid designed and fabricated earlier in the program. Six of the eleven functional S/Hs identified at wafer level were subsequently tested in the high frequency package.

The dynamic performance of one of the HBT S/Hs is illustrated in Figure 5. This S/H uses 7 x 7 μm^2 emitter bipolar HBT devices everywhere except for the sampling gate, which uses 5 x 5 μm^2 Schottky diodes. Each photo shows the output of the S/H with the S/H clock waveform (S/H tracks while the clock is high). Input signals of 50 MHz and 125 MHz are shown being sampled at a clock frequency of 500 MHz. Although the measured performance falls short of the program requirements, the results are very promising.

In addition to overall dynamic functionality, a number of specific dynamic characteristics were measured, including droop, settling, and bandwidth. The S/H droop rate during the hold mode was measured at 200 mV/ns. The droop, which varies linearly with transistor current gain, is four times the simulated value. The high droop rate is a result of low current gain on the hold amplifier input transistor. Settling response to a high edge rate pulse (200 ps 10-90% rise time) was also measured. The S/H settled to within 1.6% (six-bits) of its final value in 2 ns. The simulated settling performance of the S/H was 1.6% (six-bits) of its final value in 1.15 ns, which is within a factor of two of the measured value. The -3 dB bandwidth of the S/H was 300 MHz, which is one-third the simulated value of 1 GHz. The reduced settling performance and bandwidth of the S/H are attributed primarily to higher-than-expected transistor contact resistances.

Because of the low yield of the June lot and handling attrition, only one S/H was available for evaluation at high frequency. Therefore, it is



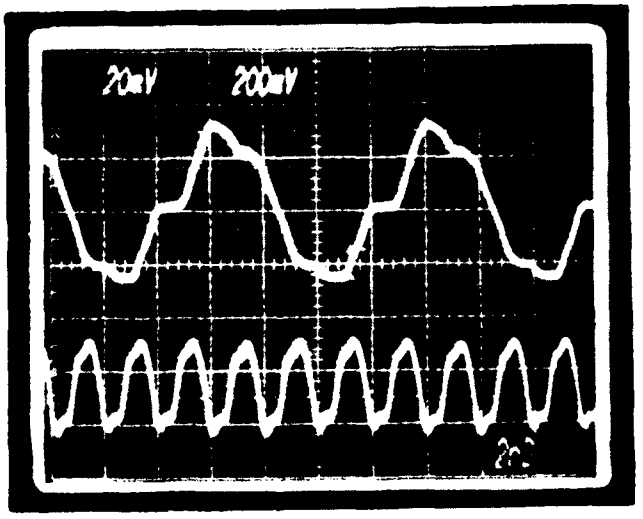


Figure 5. Dynamic performance of S/H with 500 MHz sample rate and 50 MHz and 125 MHz input video signals, respectively.

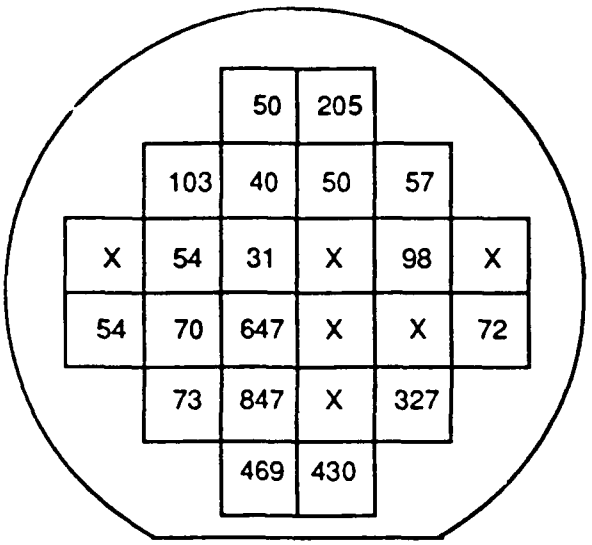
difficult to draw conclusions concerning the capabilities of the process or the circuit design based on the June lot. During the next quarter, the S/Hs from the higher-yielding August lot will be scribed and dynamically evaluated. Given the factor of 15 increase in the number of available functional ICs, a more representative dynamic characterization will be possible.

C. Device Characterization

To better understand the yield problems with the four-bit and five-bit ADCs, Hughes completed a brief dc characterization of the 7 x 7 μm^2 double base devices used throughout each design. The characterization revealed that the devices have contact resistances an order of magnitude larger than the HBT model used in the design of the two ADC chips.

Wafer maps of emitter and collector resistance from the August lot are shown in Figure 6. The emitter resistance was obtained by observing the base current as a function of collector-emitter voltage, V_{CE}, with the collector open-circuited. The measured emitter resistance (r'_e) has an average value of 196 Ω with a standard deviation of 201 Ω. The collector resistance (r'_c) was obtained by plotting the collector current I_C vs V_{CE} characteristics at constant base currents. The active or normal collector resistance was obtained by fitting a line to the "knees" of the I_C vs V_{CE} curves. The measured collector resistance has an average value of 946 Ω with a standard deviation of 1.055 kΩ.

In addition to contact resistance, current gain (β) and base-emitter voltage (V_{be}) were measured on each of the 7 x 7 μm^2 double base devices with a 1 mA emitter current. The average β was 28.2, with a standard deviation of 19.4. The average V_{be} was 1.492 V, with a standard deviation of 195 mV from site to site. From the r'_e data it is clear that V_{be} mismatch is driven predominantly by variations in emitter contact resistance. Because of wafer testing problems, no statistically meaningful die adjacent data are available for the August lot.



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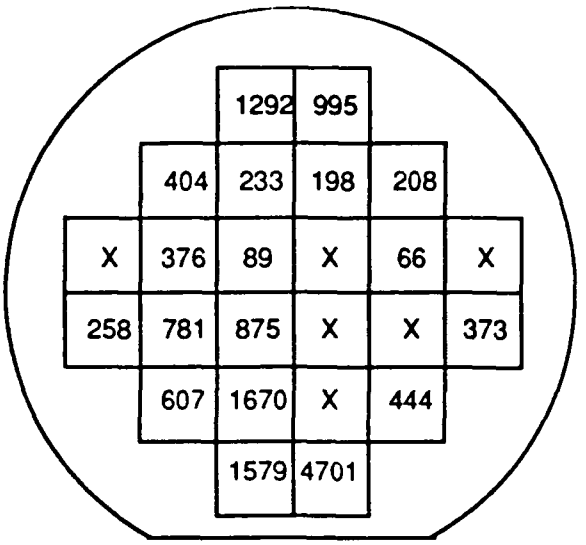

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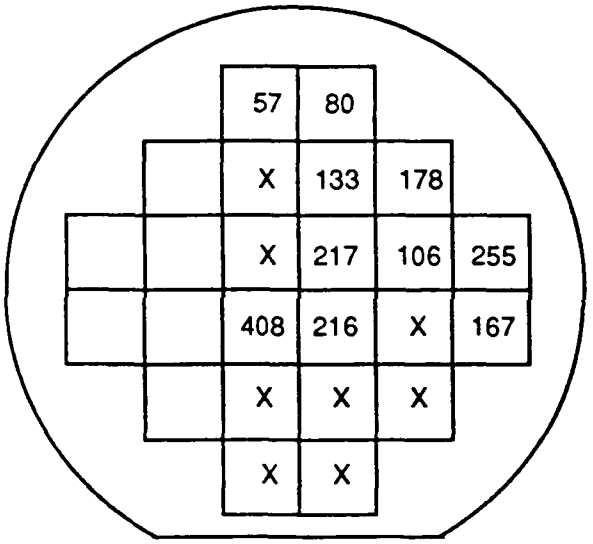

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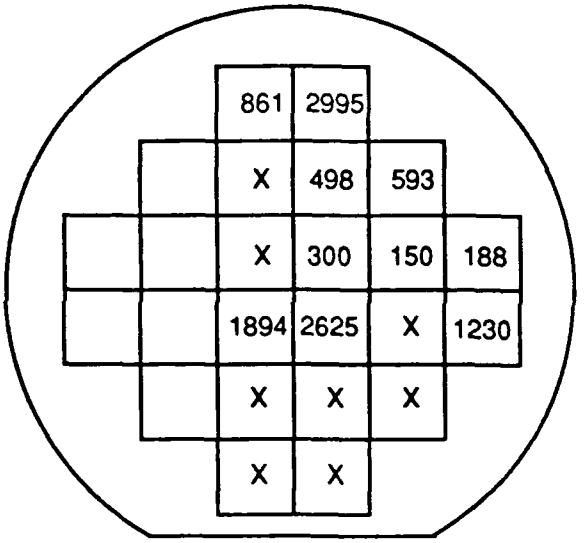

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EMITTER RESISTANCE Re

Average	**196 Ω**
Standard Dev.	**201 Ω**

COLLECTOR RESISTANCE Rc

Average	**946 Ω**
Standard Dev.	**1055 Ω**

Figure 6. Wafer maps of bipolar HBT emitter and collector contact resistances, R_e and R_C (7 x 7 μm^2 double base device).

D. Circuit Design

Hughes completed circuit simulations of the four-bit and five-bit ADC designs to determine their sensitivity to high HBT contact resistances. The simulations predicted that an emitter resistance of 150 Ω would reduce the gain of the ADC circuits such that no bit switching would take place. High emitter resistance (≥ 150 Ω) would therefore reduce the ADC functional yield to 0%. In addition, the high collector resistance of the HBT devices would tend to substantially forward bias (1 V to 2 V) the collector-base junction of most of the transistors in the design, further hindering proper dc circuit operation.

The HBT model parameters for r_e and r_c used in the design of the four-bit and five-bit ADCs were 17 Ω and 42 Ω, respectively, an order of magnitude lower than the measured parameters (7 x 7 μm^2 emitter with double base). Hughes believes that target upper bound values of r_e = 200 Ω and r_c = 400 Ω can be tolerated if the ADC circuits are redesigned. Although site-to-site variations in r_e and r_c are less problematic, die-adjacent transistor contact matching (specifically, r_e) must be kept better than 25% for the differential circuits to operate properly. Obviously, as the ratio between the contact resistances and the circuit load resistances improves, the percent matching requirement can be relaxed. Die-adjacent transistor contact values of 20 Ω ± 10% and 50 Ω ± 50% for r_e and r_c, respectively, should be the goals for high speed, high accuracy circuit performance.

To improve the yield of the four-bit and five-bit ADCs, Hughes will redesign both ICs for improved sensitivity to high device contact resistances. Although the redesign will significantly affect the maximum sample frequency of the ADCs, the sensitivity to contact resistance will be substantially reduced. The redesigned five-bit test bar mask set is targeted for release in early November.

Deficiencies in the HBT process are expected to cause significant slips in the release of the 8-bit and 12-bit mask sets.

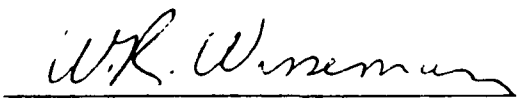
E. Plans For Next Quarter

1. Solve high contact resistance problem.

2. Redesign five-bit ADC test bar mask set for improved sensitivity to high HBT device contact resistances.

3. Complete dynamic characterization of S/H circuits from August lot.

4. Begin system design for 12-bit ADC.



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